# Effects of Varying the Fin Width, Fin Height, Gate Dielectric Material, and Gate Length on the DC and RF Performance of a 14-nm SOI FinFET Structure"

**Authors:** **Nour El I. Boukortt,** Trupti Ranjan Lenka, Salvatore Patanè, Giovanni Crupi
Journal**:** State-of-the-Art Nanoscale Electronic and Photonic Devices

Received: 14 November 2021 / Revised: 25 December 2021 / Accepted: 26 December 2021 / Published: 28 December 2021

**Abstract**

The FinFET architecture has attracted growing attention over the last two decades since its invention, owing to the good control of the gate electrode over the conductive channel leading to a high immunity from short-channel effects (SCEs). In order to contribute to the advancement of this rapidly expanding technology, a 3D 14-nm SOI n-FinFET is performed and calibrated to the experimental data from IBM by using Silvaco TCAD tools. The calibrated TCAD model is then investigated to analyze the impact of changing the fin width, fin height, gate dielectric material, and gate length on the DC and RF parameters. The achieved results allow gaining a better understanding and a deeper insight into the effects of varying the physical dimensions and materials on the device performance, thereby enabling the fabrication of a device tailored to the given constraints and requirements. After analyzing the optimal values from different changes, a new device configuration is proposed, which shows a good improvement in electrical characteristics.